

Chameleon: a Heterogeneous and Disaggregated Accelerator System for Retrieval-Augmented Language Models

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Abstract

A Retrieval-Augmented Language Model (RALM) augments a large language model (LLM) by retrieving context-specific knowledge from an external database via vector search. This strategy facilitates impressive text generation quality even with smaller models, thus reducing computational demands by orders of magnitude. However, RALMs introduce unique system design challenges due to (a) the diverse workload characteristics between LLM inference and retrieval and (b) the various system requirements and bottlenecks for different RALM configurations including model sizes, database sizes, and retrieval frequencies. We propose *Chameleon*, a heterogeneous accelerator system integrating both LLM and retrieval accelerators in a disaggregated architecture. The heterogeneity ensures efficient serving for both LLM inference and retrieval, while the disaggregation allows independent scaling of LLM and retrieval of accelerators to fulfill diverse RALM requirements. Our Chameleon prototype implements retrieval accelerators on FPGAs and assigns LLM inference to GPUs, with a CPU server orchestrating these accelerators over the network. Compared to CPU-based and CPU-GPU vector search systems, Chameleon’s retrieval accelerators achieve up to 23.72× speedup and 26.2× energy efficiency. Evaluated on various RALMs, Chameleon exhibits up to 2.16× reduction in latency and 3.18× speedup in throughput compared to the hybrid CPU-GPU architecture. These promising results pave the way for adopting accelerator heterogeneity and disaggregation into future RALM systems.

1 Introduction

The recent advances in generative large language models (LLMs) are attributable to the surging number of model parameters trained on massive datasets [12, 21, 86, 96]. The intuition behind the scaling-up approach is to leverage more model parameters to learn and encapsulate textual knowledge, thus offering more precise and informed responses.

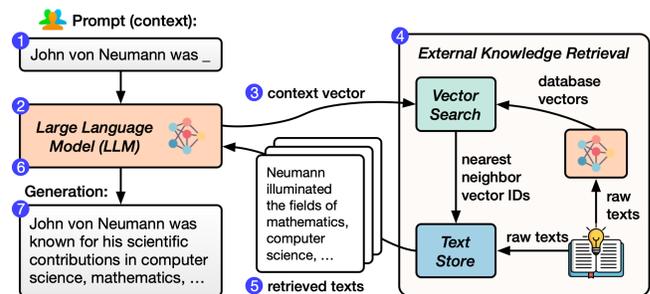


Figure 1. A retrieval-augmented language model (RALM).

However, improving LLM quality by scaling up models leads to three major problems. Firstly, the increased computational demands result in higher inference costs [9, 12]. Secondly, updating knowledge in the LLM is inflexible: the latest information, like recent news, is not incorporated without additional training, and removing harmful or sensitive data, such as personal information mistakenly included in the training set [13, 100], can be difficult, often requiring the model to be retrained from scratch [11, 14]. Finally, the reliability of LLMs is still a matter of concern, as they may produce non-factual content [69, 72] without adequately learning or applying knowledge pertinent to the context.

Retrieval-Augmented Language Models (RALMs) effectively addresses the aforementioned problems. In RALM, the LLM focuses on learning linguistic structures, while context-specific knowledge is incorporated during inference. Figure 1 overviews the RALM architecture. The external knowledge database encodes textual knowledge into vectors using LLMs and stores them in a vector database. During inference, the knowledge retriever identifies relevant knowledge in the database via vector search, which assesses relevance by computing the

similarity between the context vector and the database vectors. Since knowledge is primarily retrieved rather than encoded in the LLM’s parameters, RALMs, even with LLMs of one to two orders of magnitude fewer parameters, can achieve superior or comparable performance to conventional LLMs on various natural language processing (NLP) tasks [34, 43, 57–59, 68, 69], thus significantly lowering the compute costs during inference. Additionally, knowledge editing can be achieved by simply updating the database, without retraining the LLM. Moreover, RALMs can produce tailored sequences by accessing private knowledge databases without including the private data in the LLM’s training corpus, a strategy recently employed by OpenAI [2, 3].

Despite its advantages, efficient RALM inference presents two challenges. *First*, the workload characteristics of the LLM and the retriever are distinct. While the LLM inference primarily relies on rapid tensor operations, the retrieval system – often utilizing fast search algorithms like Product Quantization (PQ) [47] – demands both substantial memory capacity for the vector database and fast processing of quantized database vectors during query time. Unfortunately, neither GPUs nor CPUs are ideal for large-scale vector search. GPUs can be cost-prohibitive for vector search at scale due to the limited memory capacity per device. Moreover, the GPU architecture is not tailored for vector search, thus the effective throughput for scanning quantized database vectors is significantly lower than the GPU memory bandwidth. Although CPUs can be coupled with abundant DRAM, they are too slow to evaluate distances between query vectors and quantized database vectors, given the intensive cache accesses and instruction dependencies during a search. *Second*, the diverse range of RALM configurations leads to shifting system requirements and bottlenecks. Various model sizes, database sizes, and retrieval frequencies can be used in a RALM, each introducing unique requirements for LLM inference performance, retrieval performance, and memory capacity needed for the database.

We envision a high-performance and efficient RALM system to adhere to two key design principles. According to Amdahl’s law, performance gains achieved by accelerating one of the RALM components, whether LLM inference or vector search, are limited by the proportion of execution time of that component. Thus, the first design principle we propose is to incorporate *heterogeneous accelerators* tailored for both RALM components rather than only employing inference accelerators such as GPUs. Secondly, the heterogeneous accelerators should be *disaggregated* to support diverse RALM demands efficiently, in contrast to a monolithic approach where a fixed number of LLM and retrieval accelerators reside on the same server. The rationale is twofold: (a) performance bottlenecks vary between different RALMs, with some demanding frequent retrieval from large databases, while others are mainly limited by the LLM inference performance, thus requiring a model-specific optimal balance

between the two types of accelerators; and (b) a huge vector database may necessitate more retrieval accelerators than a single server can accommodate.

To materialize this vision, we propose *Chameleon*, a heterogeneous and disaggregated accelerator system for efficient, flexible, and high-performance RALM inference. Chameleon consists of three primary components. Firstly, *ChamVS* is a distributed and accelerated vector search engine. It consists of several disaggregated memory nodes, each containing a shard of quantized database vectors in DRAM, a near-memory retrieval accelerator prototyped on FPGA, and a hardware TCP/IP stack. Secondly, *ChamLM* is a multi-GPU LLM inference engine. It produces query vectors and generates texts using the retrieved information. Lastly, a CPU coordinator server orchestrates the network communication between the retrieval and LLM accelerators.

We evaluate Chameleon with different LLM architectures, LLM sizes, database sizes, and retrieval frequencies. For large-scale vector search, ChamVS achieves up to 23.72× latency reduction compared to the state-of-the-art CPU-based systems while consuming 5.8~26.2× less energy per query. For RALM inference, Chameleon achieves up to 2.16× speedup in latency and 3.18× increase in throughput compared to the hybrid CPU-GPU architecture. We further illustrate that the optimal balance between the two types of accelerators varies significantly across different RALMs, making disaggregation essential for achieving both flexibility and high accelerator utilization rates. The impressive performance and flexibility of Chameleon encourage future RALM systems to adopt such a heterogeneous and disaggregated design.

Contributions:

- We present Chameleon, an efficient RALM inference system that combines two proposed design principles: accelerator heterogeneity and disaggregation.
- We design and implement ChamVS, a distributed engine for large-scale vector search, which includes:
 - Disaggregated memory nodes accelerated by near-memory vector search processors.
 - A novel hardware design for fast top-K selection while consuming minimal hardware resources.
 - A GPU-based index scanner to prune search space.
- We evaluate Chameleon on various RALMs and showcase its remarkable performance and efficiency.

2 Background and Motivation

2.1 Retrieval-Augmented Language Models

A RALM combines a transformer-based LLM [23, 85, 87] with an external knowledge database. During inference, information relevant to the current context is retrieved from the database and utilized by the LLM to predict subsequent tokens. We classify RALMs by the content they retrieve:

The first category of RALMs retrieves *text chunks* containing multiple tokens related to the current context. Popular examples of this category employ the *encoder-decoder* transformer architecture [10, 43, 69], as the decoder-only models are less flexible in integrating text chunks [88]. The encoder-decoder model comprises two primary components: an encoder, responsible for processing retrieved texts, and a decoder, which produces output tokens. During inference, initial states, such as a user’s prompt, are vectorized to retrieve context-related knowledge, i.e., text chunks in the database with similar vector representations [10, 44, 69]. The retrieved text chunks are then concatenated and processed by the encoder, and their latent knowledge representations are conveyed to the decoder via the cross-attention mechanism [98], leading to the generation of output tokens. When generating long sequences, however, the generated content may gradually diverge from the initially retrieved contents. Thus, instead of initiating retrieval only once at the beginning [43, 69, 91], an effective strategy is to perform multiple retrievals during text generation to improve token generation quality [88], for instance, at a regular interval of every 64 generated tokens [10].

The second category of RALMs retrieves only the *next token* of each similar context in the database. These RALMs employ a *decoder-only* model [6, 58, 78]. At each step of token generation (retrieval interval is one), the last layer’s hidden state serves as the query to retrieve similar contexts and the next token of each similar context [58, 78, 103]. The next token of the current context is then predicted by interpolating the next-token probability distribution predicted by the model with that of the retrieved content [57, 58].

From a performance standpoint, the two categories differ in two aspects. Firstly, regarding retrievals, the latter category retrieves every step of token generation (higher retrieval cost), while the former category may either employ multiple-token intervals or retrieve just once at the beginning per sequence. Secondly, in terms of computation, the former category, which often adopts the encoder-decoder architecture, introduces the cost of encoder inference per retrieval step and cross-attentions between decoder and encoder every token generation step (higher computational cost), while the latter category, with a decoder model, only requires an extra interpolation of the next token’s probability distribution, introducing minimal computational overhead.

2.2 Large-Scale Vector Search

A vector search takes a D -dimensional query vector x as input and retrieves K similar vector(s) from a database Y , populated with many D -dimensional vectors, based on metrics like L2 distances. While the nearest neighbor search retrieves the exact K closest vectors, linearly scanning through a large vector set can be prohibitively expensive. Thus, real-world vector search systems adopt approximate nearest neighbor (ANN) search that trades accuracy for much higher system

Table 1. Definitions of important symbols in IVF-PQ.

Symbol	Definition
x	A query vector.
y	A database vector.
m	The sub-space number of product quantization.
$nlist$	The number of clusters in the IVF index.
$nprobe$	The number of IVF lists to scan per query.
K	The number of nearest neighbors to return.

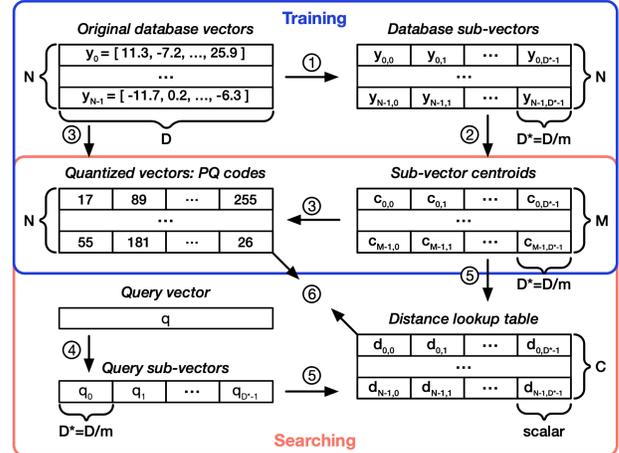


Figure 2. Product quantization (PQ) for vector search.

performance. The quality of an ANN search is measured by the recall at K ($R@K$), which denotes the overlap percentage between the exact K nearest neighbors and the K returned by the ANN. In the subsequent sections, we will use the terms *vector search* and *ANN search* interchangeably.

IVF-PQ is currently the most popular vector search algorithm in RALMs [10, 43, 58, 69] thanks to its great performance in large-scale ANN search [32, 47, 52]. IVF-PQ combines (a) an inverted-file (IVF) index to prune the search space and (b) product quantization (PQ) to compress database vectors and reduce the computational demands during the search process. Table 1 shows key parameters in IVF-PQ.

Inverted-File (IVF) Index. An IVF index divides a vector dataset Y into many ($nlist$) disjoint subsets, typically using clustering algorithms like K-means. Each of these subsets is termed an IVF list. At query time, the IVF index is scanned, and only a select few ($nprobe$) IVF lists whose cluster centroids are close to the query vector are scanned, such that the search space is effectively pruned.

Product Quantization (PQ). PQ reduces memory usage and computational requirements of vector search by compressing each database vector into m -byte PQ codes. The training and searching workflow of PQ is shown in Figure 2.

To quantize database vectors, all database vectors are partitioned evenly into m sub-vectors ①. Each sub-vector possesses a dimensionality of $D^* = \frac{D}{m}$, typically ranging from 4

to 16 in practice. A clustering algorithm is performed in each sub-space ② and results in a list of centroids c , allowing each database sub-vector to be approximated by its nearest centroid. Typically, the number of clusters per sub-space is set as $M = 256$, such that a cluster ID can be represented with one byte. Thus, once the cluster centroids are stored, each database vector can be represented by m -byte PQ codes.

During the search process, a query vector will be compared against the quantized database vectors. The distance computation can be formulated as $\hat{d}(x, y) = d(x, c(y)) = \sum_{i=1}^m d(x_i, c_i(y_i))$, where $\hat{d}(x, y)$ is the approximate distance between a query vector x and a quantized database vector y , and $c(y)$ is the reconstructed database vector using the PQ codes and the cluster centroid vectors per sub-space. To calculate $\hat{d}(x, y)$, the query vector is divided into m sub-vectors (x_i) ④ and compared against the reconstructed quantized sub-database-vectors $c_i(y_i)$. To speed up distance computations with many database vectors, it would be beneficial to construct a distance lookup table ⑤ that can be reused within a query, encompassing all combinations between a sub-query-vector and a cluster centroid within the same sub-space. With this table, the value of $d(x_i, c_i(y_i))$ can be swiftly retrieved by looking up the table with the PQ code as the address ⑥, leading to improved computational efficiency.

2.3 Motivation: Efficient RALM Inference

An efficient RALM inference engine should meet the following **system requirements**:

- Both the LLM inference and the large-scale vector search components should be fast and resource-efficient.
- The system should be flexible enough to accommodate diverse RALM configurations, spanning various combinations of (a) transformer architectures, (b) model sizes, (c) database sizes, and (d) retrieval frequencies.

However, little effort has been devoted to developing efficient RALM systems that meet the above requirements. This is likely because RALM has been an emerging topic within the machine learning community. Specifically, the current RALM systems employed in machine learning research [10, 43, 44, 58, 69] exhibit the following shortcomings:

First, each research RALM system focuses on *being able to run* one or a small number of RALM models, paying little attention to performance, resource efficiency, and system adaptability for diverse RALM configurations.

Second, while hardware accelerators for LLMs, such as GPUs, are advancing rapidly, less attention has been paid to the retrieval aspect, which, as our evaluations will demonstrate, can become the performance bottleneck in RALM inference because neither CPUs nor GPUs are the ideal processors to search on such a vast volume of vector data.

On the one hand, CPUs are slow in scanning PQ codes during query time ⑥. This inefficiency arises due to the frequent cache accesses (for each byte of PQ code, load the code

and use it as an address to load a distance) and the instruction dependencies between operations (distance lookups depend on PQ codes and distance accumulations depend on the lookup values). Even utilizing the state-of-the-art SIMD-optimized CPU implementation [1], the throughput peaks at roughly 1 GB/s per core when scanning PQ codes (1.2 GB/s on Intel(R) Xeon(R) Platinum 8259CL @ 2.50GHz). Within a core-memory-balanced server, the PQ code scanning process significantly underutilizes the available memory bandwidth, as about 16 cores are required to saturate the bandwidth of a single memory channel (around 20 GB/s).

On the other hand, GPUs present two primary limitations for large-scale vector search. Firstly, the limited memory capacity of individual GPUs makes large-scale searches on GPU clusters cost-prohibitive. For instance, accommodating only 1 TB of PQ codes would necessitate at least 16 NVIDIA A100 GPUs, each with 80 GB of memory, given that a portion of memory should be reserved for intermediate states during the search. These GPUs cost 300K USD in total¹ excluding the host servers. Although an alternative solution is to adopt a hybrid CPU-GPU architecture where the GPU fetches vectors from CPU’s memory, the inter-processor bandwidth is way lower than the GPU memory bandwidth. Even for NVIDIA Grace Hopper, with the latest high-performance CPU-GPU interconnect, the single-direction bandwidth of 450 GB/s is only 15% of the GPU’s bandwidth. Secondly, the throughput for PQ code scanning on GPUs is considerably lower than the GPU’s bandwidth, only around 50% of the bandwidth even with large batch sizes (evaluated on NVIDIA V100), due to the multiple passes of memory accesses to write and read intermediate results at each search step [52]. Thirdly, the many cores in GPUs are underutilized due to the low computational intensity of scanning PQ codes, but they still incur static power consumption.

3 Chameleon: System Overview

We present Chameleon, a heterogeneous and disaggregated accelerator system for efficient, flexible, and high-performance RALM inference. **Chameleon addresses the system challenges in RALMs in the following ways:**

- Chameleon employs heterogeneous hardware to accelerate both LLM inference and vector search efficiently.
- Chameleon disaggregates the accelerators, enabling independent scaling for each type of hardware, thus supporting various RALM configurations efficiently.
- Chameleon’s modular design allows flexible hardware upgrades in the future, such as integrating more powerful LLM inference accelerators or ASIC-based ChamVS retrieval accelerators.

Figure 3 overviews the Chameleon architecture, which primarily consists of the following components.

¹Price on amazon.com as of October 2023.

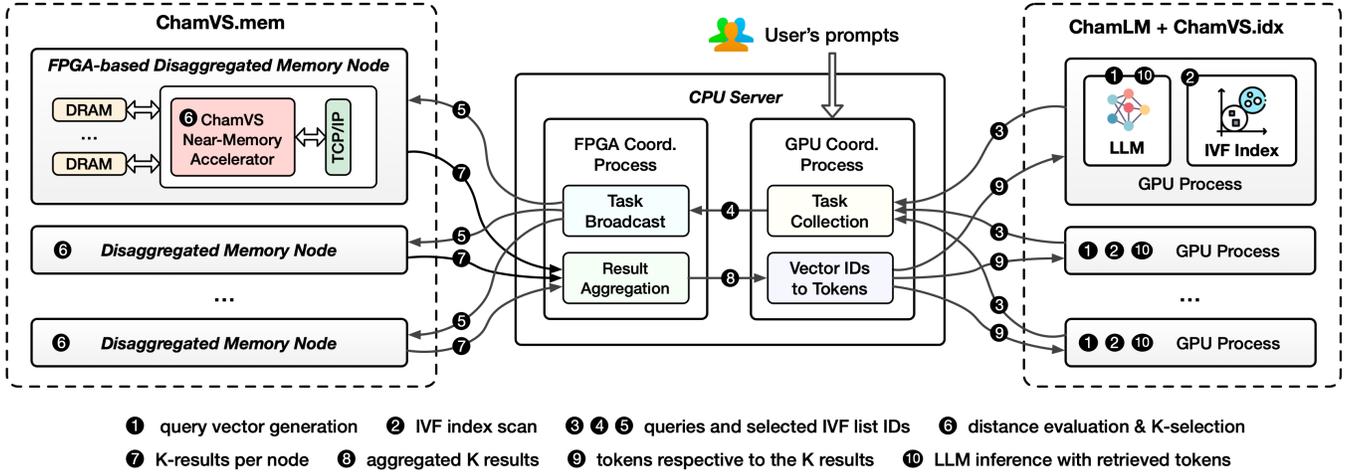


Figure 3. Chameleon is a heterogeneous and disaggregated accelerator system for efficient RALM inference.

Firstly, ChamLM is a multi-GPU LLM inference engine, as shown on the right side of Figure 3. Each GPU is managed by an independent GPU process. These processes can reside on either the same or different servers. As introduced in Section 2.1, even small LLMs, typically fit within a single GPU, can achieve high-quality generation when integrated with retrieval [10, 69]. Consequently, ChamLM assigns each GPU a copy of the entire LLM, while larger models in the future can be implemented by simply extending ChamLM to support model parallelism across GPUs.

Secondly, ChamVS is a distributed accelerator engine for low-latency vector search. On the one hand, ChamVS.idx is a GPU-based IVF index scanner colocated with the ChamLM GPUs (right side of Figure 3). While the index scan can be executed on CPUs or FPGAs, GPUs are generally more favorable for handling such an embarrassingly parallel workload due to their superior memory bandwidth and computational capability. Given that GPUs are already integrated into Chameleon, no additional devices are required. The only overhead is a minimal increase in GPU memory usage, because the index sizes, typically under one GB, are small enough compared to the vast memory footprints of the database vectors. On the other hand, ChamVS.mem is responsible for querying quantized database vectors. ChamVS.mem contains one or multiple disaggregated memory nodes, each with a partition of the database vectors and a near-memory retrieval accelerator prototyped on FPGA for query processing (left side of Figure 3).

Thirdly, a CPU server manages the lightweight communication between the GPUs and FPGAs. After receiving search requests from the GPU processes, it dispatches them to the FPGA-based disaggregated memory nodes, aggregates the per-partition results returned by the FPGAs, converts the K nearest neighbor vector IDs into their corresponding texts, and sends the retrieved tokens back to the GPUs. Since each

query only requires less than ten KBs of network data transfer, the communication latency is negligible compared to vector search and LLM inference.

Token generation workflow. For each token generation step, the procedure diverges depending on whether the retrieval is invoked. Without retrieval, the GPUs infer the next token as in regular LLMs. With retrieval, the first step is to generate a contextual query vector ❶, either by using the hidden state of the current context [57, 58] or encoding the query tokens through another model [10]. Following this, the IVF index residing on the same GPU is scanned to select the *nprobe* most relevant IVF lists ❷. The query vector and the list IDs are then transmitted to the GPU coordinator process running on the CPU node via the network ❸. After recording the association between queries and GPU IDs, the query and list IDs are forwarded to the FPGA coordination process ❹, which broadcasts them to the FPGA-based disaggregated memory nodes ❺. The ChamVS near-memory processor on each node then uses the query vectors to construct distance lookup tables for each IVF list, computes the distances between the query and quantized database vectors, and collects the K nearest neighbors ❻. Subsequently, the result vector IDs and distances from all memory nodes are sent back to the CPU server ❼, which aggregates the results ❽ and returns the tokens of the nearest neighbors to the originating GPU ❾. Finally, the GPU predicts the next token based on both the context and the retrieved tokens ❿.

4 ChamVS Near-Memory Accelerator

ChamVS enables high-performance, large-scale vector search by pairing each disaggregated memory node with a near-memory accelerator. Figure 4 shows the architecture design of the retrieval accelerator, applicable to not only FPGAs but also future ASICs. The accelerator comprises a distance lookup table construction unit, several PQ decoding units

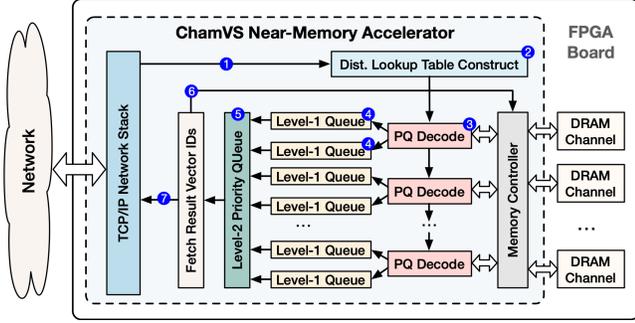


Figure 4. The ChamVS near-memory retrieval accelerator.

for distance evaluation between query vectors and quantized database vectors, a group of systolic priority queues for parallel K -selection, and multiple memory channels. In this section, we mainly elaborate on the PQ decoding units and the K -selection circuit, omitting the distance lookup table construction unit since it simply calculates L2 distances.

4.1 PQ Decoding Units

A PQ decoding unit reads quantized database vectors (PQ codes) from DRAM and computes the corresponding L2 distances to query vectors using a distance lookup table.

Figure 5 presents the design of a single PQ decoding unit, which can produce a result distance every clock cycle. We adopt a design with operator and pipeline parallelisms similar to [50, 65]. For each IVF list to scan, the unit first stores the input distance lookup table in BRAM (on-chip SRAM in FPGAs). The shape of the lookup table is $m \times 256$ for the typical 8-bit PQ codes ($2^8 = 256$), where m is the number of bytes per quantized vector. Different table columns are stored in separate BRAM slices, facilitating parallel distance lookups. Subsequently, the database PQ codes are loaded from DRAM and streamed to the PQ decoding unit via an m -byte-wide FIFO, with each byte serving as an address to retrieve a value from the corresponding column of the table. Upon completion of the m parallel table lookup operations, an adder tree sums up the values to produce the approximate distance between the query vector and the quantized database vector. The lookup and addition processes are pipelined such that the unit can consistently process m bytes of PQ codes and yield a result each clock cycle.

Multiple PQ decoding units operate in parallel to fully utilize the memory bandwidth, as shown in Figure 4 ③. When scanning a cluster of vectors, all units share the same distance lookup table, as each cluster is equally distributed across all memory channels. The units are arranged in a one-dimensional array, enabling each unit to forward the table to the subsequent one. This arrangement avoids a broadcasting topology, thus mitigating potential wire routing issues.

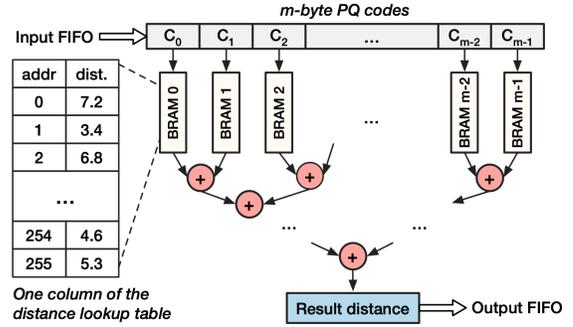


Figure 5. The architecture design of a PQ decoding unit.

Summary: The parallelism both across and within PQ decoding units enables rapid distance computations between query vectors and quantized database vectors.

4.2 Efficient K -Selection Module

Designing an efficient K -selection microarchitecture within ChamVS.mem is challenging, as each PQ decoding unit generates one distance every clock cycle, requiring the K -selection module to manage multiple incoming elements per cycle. In this section, we begin by examining the register-array-based systolic priority queue, a building block for the K -selection module. However, instantiating many systolic priority queues of length K to satisfy throughput requirements proves too costly due to prohibitively high hardware resource consumption. Consequently, we propose the approximate hierarchical priority queue, a high-throughput, resource-efficient design for parallel K -selection on hardware.

4.2.1 Primitive: Systolic Priority Queue. Figure 6 shows the systolic priority queue [41, 66] for high-throughput input ingestion. It comprises a register array interconnected by compare-swap units, repeating a two-cycle procedure for each input. During an odd cycle, the leftmost node is replaced with the minimum value between the existing leftmost value and the input, followed by the compare-and-swap operations of all even entries in the array with their corresponding odd neighbors. In the subsequent cycle, the compare-and-swap operation is applied between odd and even entries. Throughout this process, the smallest element is gradually swapped to the rightmost position in the queue. The hardware resource consumption of such a priority queue scales linearly with its length, as both the number of registers and compare-swap units are proportional to the queue size.

A natural approach to implement K -selection in ChamVS is to instantiate a group of systolic priority queues in a hierarchical structure, as shown in Figure 4 ④⑤. Since a systolic priority queue can only ingest one input every two cycles, two queues, termed as level-one (L1) queues, should be paired with one PQ decoding unit, as it can produce one output per cycle. For each query, each L1 queue collects a subset of the K

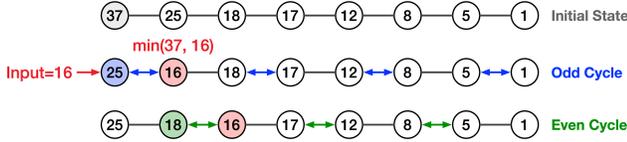


Figure 6. The systolic priority queue architecture.

nearest neighbors, and the level-two (L2) queue subsequently selects the final K results.

Unfortunately, a straightforward implementation of the hierarchical priority queue can consume an excessive amount of hardware resources, making the solution unaffordable even on high-end FPGAs. For example, a 100-element priority queue would utilize around 2.5% of lookup tables (LUTs) on the Alveo U250, one of AMD’s largest FPGA models. Given 32 instantiated PQ decoding units, the accelerator would necessitate 64 L1 queues to match the throughput of the decoding units, an amount that already exceeds the total LUT resources available on the FPGA. Consequently, it becomes imperative to devise a more resource-efficient approach for K -selection.

4.2.2 Approximate Hierarchical Priority Queue. We propose the approximate hierarchical priority queue architecture for high-performance and resource-efficient K -selection. Recognizing that the approximate nearest neighbor search inherently does not yield exact results, we relax the K -selection objective from selecting the K smallest distances in all queries to collecting precise results in the vast majority of cases, such as in 99% of the queries.

The intuition behind the approximate K -selection design is simple: it is unlikely that all the K results are produced by a single PQ decoding unit. For example, given 16 level-one queues with $K = 100$, the average number of the top 100 results in a queue is $100/16 = 6.25$. More specifically, the probability that one queue holds k of the K nearest neighbors can be formulated as $p(k) = C_K^k * (\frac{1}{num_queue})^k * (1 - \frac{1}{num_queue})^{K-k}$, where C_K^k represents the number of combinations selecting k out of K items. The cumulative probability that a queue contains no more than k of the K results can be calculated by $P(k) = \sum_{i=0}^k p(i)$. The probability distribution of p and P are visualized by the red bars and the blue curve in Figure 7, respectively. The figure demonstrates that it is highly unlikely that a queue holds more than 20 out of the $K=100$ results; thus, the length of the L1 priority queue can be truncated to 20 while producing almost the same results.

Our design aims to reduce the size of the L1 queues while ensuring that the results for 99% of queries remain identical to those obtained with an exact K -selection module. Specifically, for 99% of the queries, none of the L1 queues will omit any result that is supposed to be returned to the user.

Figure 8 shows the resource savings achieved by applying the approximate hierarchical priority queue. As the number

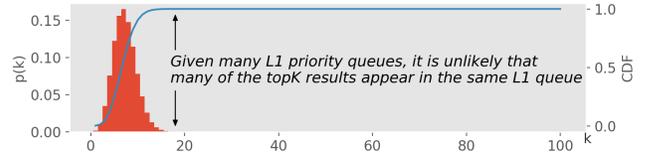


Figure 7. The probability distribution that one out of the 16 L1 priority queues holds k out of the 100 nearest neighbors.

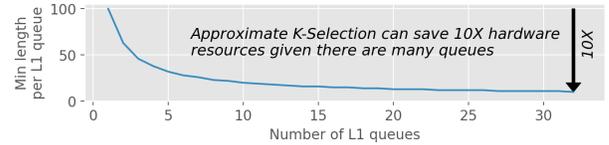


Figure 8. The proposed approximate hierarchical priority queue can save hardware resources by an order of magnitude.

of L1 queues increases, the queue sizes can be reduced by an order of magnitude while still retaining 99% of identical results. As the resource consumption of a queue is almost proportional to its length, such a reduction in size leads to a corresponding decrease in hardware resource consumption.

Summary: The approximate hierarchical priority queue architecture, by reducing each queue’s size, can match the high throughput of PQ decoding units and significantly lower hardware resource consumption.

4.3 Memory Management

ChamVS.mem directly manages the physical address space to avoid memory virtualization overheads. Specifically, the PQ codes and vector IDs are in DRAM, while the metadata is loaded into BRAM during system initialization. The metadata includes (a) an address lookup table recording the starting physical address of PQ codes and vector IDs of each cluster and (b) the centroid vectors of the product quantizer.

ChamVS evenly distributes query workloads across memory nodes and channels. A large vector dataset is first segmented into equal-sized partitions for each memory node. Assuming a similar data distribution across partitions, each node would hold a comparable number of vectors per IVF list, leading to balanced query workloads per node. Further, within each memory node, each IVF list is evenly distributed among all memory channels, thereby achieving workload balance across these channels as well.

Summary: ChamVS’s memory management mechanism avoids virtualization overheads and balances workloads across memory nodes and channels.

Table 2. Various RALM configurations in the evaluation.

	Dim.	Layers	Heads	Param.	Interval	K
Dec-S	512	24	8	101M	1	100
Dec-L	1024	96	16	1259M	1	100
EncDec-S	512	2,24	8	158M	8/64/512	10
EncDec-L	1024	2,96	16	1738M	8/64/512	10

5 Implementation

Chameleon is implemented in 11K lines of code in total, including 3K lines of Vitis HLS C/C++ for the near-memory accelerator, 1.4K lines of C++ for the CPU coordination programs between GPUs and FPGAs, 3.5K lines of Python for the LM inference engine with the retrieval interface, and 3.2K lines of Python for various experiments and tests.

ChamLM. Referring to existing RALM research projects [57, 58], we build ChamLM on top of Fairseq [81], a language model toolkit based on PyTorch [82] that allows flexible instantiation of different LLM architectures and parameters. ChamLM extends Fairseq to support functionalities such as multi-GPU inference, initiating retrieval requests, integrating the retrieved tokens into the models, and TCP/IP network communication between the vector search engines and different GPU processes.

ChamVS. For ChamVS.idx, we use Faiss [52] to support such efficient index scan on both CPUs and GPUs. We develop the ChamVS near-memory accelerator using Vitis HLS 2021.2 in C/C++ and integrate an open-source FPGA TCP/IP network stack [37] that connects to the accelerator kernel. The coordinator process between ChamVS.idx and ChamVS.mem for query broadcasting and result aggregation is implemented using C/C++ and the socket library.

6 Evaluation

We evaluate Chameleon to answer the following questions:

1. How much performance and energy benefits can ChamVS attain in large-scale vector search? (§ 6.2)
2. How does Chameleon perform across different RALMs by introducing heterogeneous accelerators? (§ 6.3)
3. Is accelerator disaggregation necessary? (§ 6.3)

6.1 Experimental Setup

LLMs. We evaluate RALM models of similar sizes to those in existing RALM research [10, 43, 73, 91, 104], from 100 million to more than one billion parameters. For each decoder-only (Dec) and encoder-decoder (EncDec) RALM, we experiment with a smaller model (S) and a larger model (L). Table 2 summarizes the four RALMs for evaluation, including input dimensionalities, numbers of layers and attention heads, model sizes, retrieval intervals, and neighbor numbers. For encoder-decoder models, we follow [10] to use a two-layer

Table 3. The vector datasets used in the evaluation.

	Deep	SIFT	SYN-512	SYN-1024
#vec	1E+9	1E+9	1E+9	1E+9
D	96	128	512	1,024
m	16	16	32	64
$nlist$	32,768	32,768	32,768	32,768
Raw vectors (GB)	384	512	2,048	4,096
PQ and vec ID (GB)	24	24	40	72

shallow encoder and a deeper decoder, and set different retrieval intervals. For all the models, we use a vocabulary size of 50K and let them generate 512 tokens per sequence.

Vector datasets. For large-scale vector search, we use two real-world datasets and two synthetic datasets as summarized in Table 3. Specifically, the SIFT and Deep datasets are the most popular benchmarks for billion-scale ANN, each with 10K query vectors. Due to the lack of openly available vector datasets for RALM, we create two synthetic datasets by replicating each SIFT vector to the models’ dimensionalities (512 and 1024), such that they can also be used in RALM inference experiments. As a common practice, we set $nlist$, the number of clusters in the IVF index, to approximately the square root of the number of dataset vectors ($nlist=32K$). We set $nprobe$ as 32 to scan 0.1% of database vectors per query, for which high recall can be achieved on both real-world datasets (93% on Deep and 94% on SIFT for 100 nearest neighbors). We quantize the SIFT and Deep datasets to 16-byte PQ codes, while the two synthetic datasets adopt 32 and 64-byte PQ codes, respectively, due to their higher dimensionalities.

Software. For vector search, we use *Faiss* [1] (v1.7.2) developed by Meta as the baseline software. Faiss is currently the most popular PQ-based ANN library, known for its highly optimized implementations for both CPUs and GPUs. For LLM inference, we extend Fairseq [81] as introduced in § 5.

Hardware. We instantiate the ChamVS near-memory accelerator on AMD Alveo U250 FPGAs (16 nm) equipped with 64 GB of DDR4 memory (4 channels x 16 GB) and set the accelerator frequency to 140 MHz. For a fair comparison, each ChamVS memory node is compared to a CPU-based vector search system with equivalent memory capacity (64 GB) and an 8-core AMD EPYC 7313 processor (7 nm) with a base frequency of 3.0 GHz and a max turbo frequency of 3.7 GHz. We evaluate NVIDIA RTX 3090 GPUs (8nm) with 24 GB GDDR6X memory. As we will show later, ChamVS can achieve better performance and energy efficiency even if instantiated on FPGAs manufactured in an older technology.

6.2 Vector Search on ChamVS

Performance. We compare ChamVS with baseline systems on four large-scale vector datasets, each using four different configurations: searching solely on CPU (CPU), scanning the IVF index on GPU and the PQ codes on CPU (CPU-GPU), scanning the index on CPU and the PQ codes on FPGA

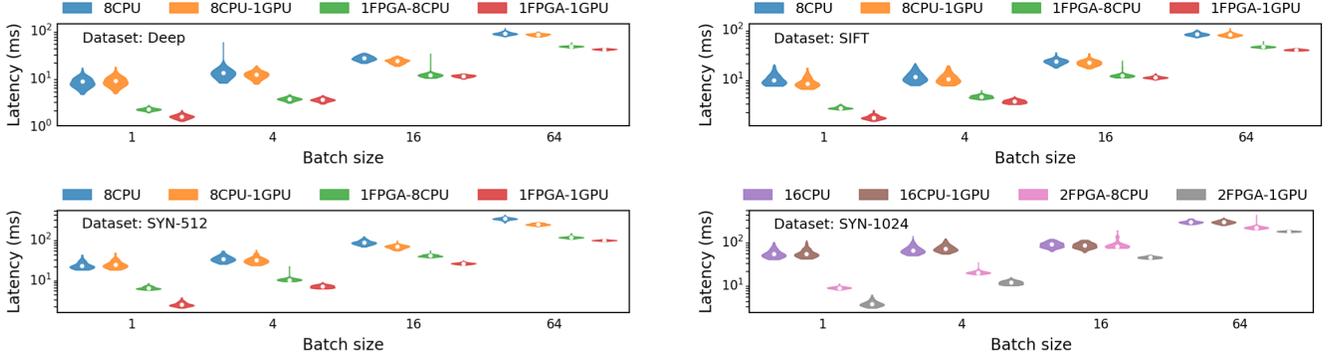


Figure 9. ChamVS achieves significantly lower vector search latency than CPUs and GPUs.

(FPGA-CPU), and scanning the index on GPU and the PQ codes on FPGA (FPGA-GPU). To report the best baseline performance, the CPU and CPU-GPU systems are monolithic, while the FPGA-CPU and FPGA-GPU systems are disaggregated over the network. Figure 9 shows the vector search latency distributions of different batch sizes using the four solutions. Each white dot in the violin plots denotes a median latency. The number of CPU cores and the number of accelerators used are listed in the plot legends. We make two primary observations from the experiments:

Firstly, the near-memory accelerator in ChamVS results in significantly lower vector search latency compared to the CPU baseline. Across different datasets and batch sizes (Figure 9), the FPGA-CPU solution achieves $1.36\sim 6.13\times$ speedup compared to the CPU baseline, and the FPGA-GPU solution shows even higher speedup ($2.25\sim 23.72\times$). This is because the ChamVS near memory accelerator can (a) decode PQ codes in parallel, (b) pipeline the decoding, distance calculation, and K-selection, such that each quantized vector can be processed by the pipeline with an initiation interval of a single clock cycle. Such specialization leads to significantly better performance compared to CPUs in scanning PQ code and selecting the K nearest neighbors.

Secondly, scanning the IVF index on GPU allows further latency improvements compared to the FPGA-CPU solution. The FPGA-GPU solution does not require additional GPUs as they are inherently available in RALM systems. As shown in Figure 9, the FPGA-GPU approach achieves $1.04\sim 3.87\times$ speedup compared to the FPGA-CPU solution. This is because the IVF index scan procedure can easily leverage the massively parallelism and the high memory bandwidth of GPUs: the query vectors are compared against all index centroid vectors, and the $nprobe$ closest centroids are selected. In contrast, the hybrid CPU-GPU solution shows little or even negative improvements compared to the CPU-only solution ($0.91\sim 1.42\times$), because the search performance is limited by the slow PQ code scan process on CPU.

Scalability. We extrapolate query latency beyond the limited number of accelerators available in our evaluation.

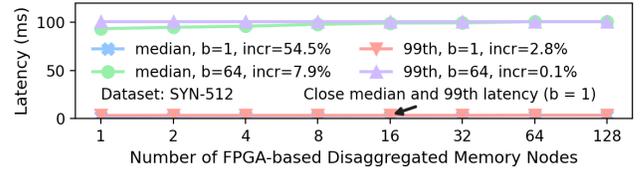


Figure 10. The query latencies for scale-out search.

Table 4. Resource consumptions of the retrieval accelerator.

Dataset	LUT	FF	BRAM	URAM	DSP
SIFT	25.3%	16.2%	13.7%	4.4%	12.2%
Deep	23.7%	15.4%	13.0%	4.4%	10.4%
SYN-512	23.2%	15.5%	23.2%	4.4%	8.4%
SYN-1024	28.0%	19.0%	35.7%	4.4%	11.9%

Considering the one-GPU and N -FPGA setup, we estimate the latency distribution by summing up accelerator and network latencies. Each query latency number is the maximum of N randomly sampled latency numbers from the 1-FPGA setup. For network latency, we assume a 100 Gbps bandwidth for the CPU server and apply the LogGP model [4, 22], which assumes a tree topology for broadcast and reduce communications, setting the latency between two endpoints as $10.0\ \mu\text{s}$ (a conservative number compared to $6.0\ \mu\text{s}$ reported in [38, 39]). Figure 10 presents the median and the 99th percentile latencies for different batch sizes on the SYN-512 dataset. The tail latencies remain almost identical to those in the one-node setup due to the negligible network latency compared to the query. As for the median latencies, there is only a 7.9% increase for a batch size of 64, while for the case without batching, the latency increases by 54.5% as the accelerator latency is determined by the slowest one.

Resource and energy consumption. For the FPGA-based near-memory accelerator, we report the resource and energy consumption using Vivado. For CPUs and GPUs, we

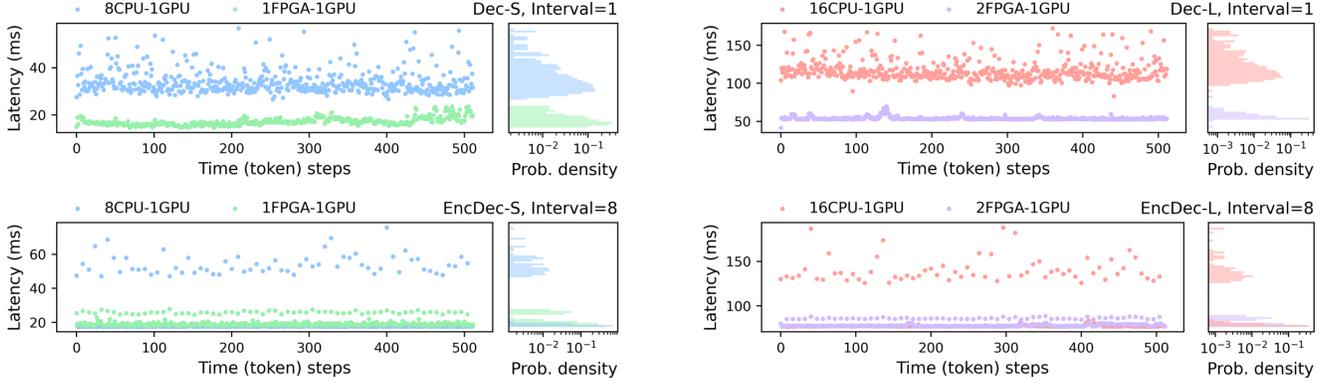


Figure 11. RALM inference latency given different LLM configurations and retrieval intervals.

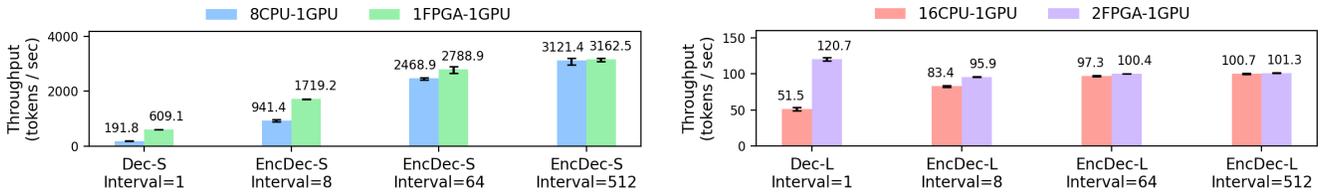


Figure 12. RALM inference throughput given different LLM configurations and retrieval intervals.

measure their energy consumption using *Intel RAPL* and *NVIDIA System Management Interface*, respectively.

The *ChamVS near-memory accelerator consumes few FPGA resources*. The AMD Alveo U250 FPGA contains 1.4M Lookup-Tables (LUTs), 2.9M Flip-Flops (FFs), 2.1K Block-RAM (BRAM), 1.3K Ultra-RAM (URAM), and 12K Digital Signal Processors (DSPs), and four memory channels. As shown in Table 4, the accelerator only consumes around 20% of the hardware resources. Considering its low hardware resource consumption, one could implement the accelerator on an FPGA with more memory channels to further improve performance and cost efficiency. For example, increasing the number of memory channels from four (as in U250) to twelve would lead to around 3× higher PQ-code scan performance.

ChamVS achieves 5.8~26.2× energy efficiency compared to the CPU. Table 5 summarizes the average energy consumption (in mJ) of different systems to serve a single query across different batch sizes. For ChamVS, we report the energy per query by measuring the power consumption times latency for scanning index on GPU and scanning PQ codes on FPGAs, respectively, and summing the two parts up.

6.3 End-to-end RALM Inference on Chameleon

In this section, we evaluate RALM inference performance on Chameleon with different model configurations and retrieval intervals. We use the SYN-512 and SYN-1024 datasets for the smaller and larger models, respectively.

Table 5. Average energy consumption per query (in mJ) on ChamVS and CPUs using various batch sizes (1~16).

	CPU			ChamVS (FPGA + GPU)		
	b=1	b=4	b=16	b=1	b=4	b=16
SIFT	950.3	434.0	143.3	53.6	28.2	21.5
Deep	929.5	412.9	141.9	52.3	26.9	20.5
SYN-512	1734.9	957.8	372.5	95.6	55.0	41.1
SYN-1024	4459.9	2315.0	918.5	170.1	107.8	85.2

Performance. We evaluate system performance when generating a 512-token sequence using a single GPU for LLM inference, and each experiment is conducted three times. For the latency evaluation, we disable batching, while for the throughput evaluation, we set the batch size as the maximum allowed given the GPU’s memory capacity (batch size = 64 for Dec-S and EncDec-S; 8 for Dec-L and EncDec-L) and assume that all sequences in the batch will finish generating 512 consecutive tokens, given that early termination for a subset of sequences can be easily addressed via preemptive scheduling [63]. For vector search in RALM, we use the FPGA-GPU solution for ChamVS and the CPU-only solution as the baseline, since the CPU-GPU vector search engine can be even slower using small batches.

Chameleon significantly outperforms the CPU-GPU baseline system in latency for inference steps involving vector search. Figure 11 compares the RALM inference latency between Chameleon (FPGA-GPU) and the baseline system

(CPU-GPU). The left column shows the small models (Dec-S and EncDec-S), while the right column shows the large models. Each row uses the same retrieval interval (one and eight). For each plot, the left subplot shows the latency over token generation steps, while the right one depicts the latency distribution. While the LLM inference is still executed on the GPU, the FPGA-GPU retrieval engine significantly reduces the latency at the token generation steps requiring retrieval. Specifically, the speedup provided by Chameleon at retrieval-based inference steps (retrieval + inference) ranges from 1.94~4.11 \times , 1.71~3.02 \times , 1.76~3.41 \times , and 1.29~2.13 \times for Dec-S, EncDec-S, Dec-L, and EncDec-L, respectively.

Chameleon achieves up to 3.18 \times throughput compared to the CPU-GPU baseline system. As shown in Figure 12, the lower the retrieval interval, the higher throughput advantage Chameleon can offer, with the speedup being 3.18 \times and 2.34 \times for Dec-S and Dec-L that require retrieval per token generation (interval = 1). Chameleon attains greater speedup in batched inference than single-sequence inference as in the latency experiments. This is because, as the batch size grows, the latency increase for LLM inference is not as significant as that of vector search, due to the many-core parallelism offered by the GPU during LLM inference. Thus, the speedup observed in batched inference is closer to that of vector search than in single-sequence inference.

The need for resource disaggregation. Given the broad range of configurations in RALMs — such as different model sizes, retrieval intervals, and database sizes — it is likely that either the LLM inference or vector search engine will be underutilized if the hardware resource ratio is not carefully configured. Based on the evaluated batched inference throughput, Figure 13 shows that the number of GPUs required to saturate the ChamVS vector search engine can vary dramatically, ranging from 0.2 to 442. This makes a monolithic design approach, which entails installing a fixed number of accelerators on a single server, both inflexible and sometimes impractical (a single server cannot accommodate 442 accelerators). Chameleon’s disaggregated architecture addresses this issue by allowing for flexible combinations of hardware resources over the network, thereby enhancing overall accelerator utilization.

In the future, ChamVS and ChamLM could be offered as distinct cloud services. This approach facilitates resource sharing among many users, thereby improving resource utilization by dynamically allocating appropriate numbers of accelerators based on real-time service demands.

7 Related Work

To the best of our knowledge, Chameleon represents the first endeavor to improve RALM inference performance from a systems perspective, addressing associated challenges via a heterogeneous and disaggregated accelerator architecture. We proceed to introduce research on related topics below.

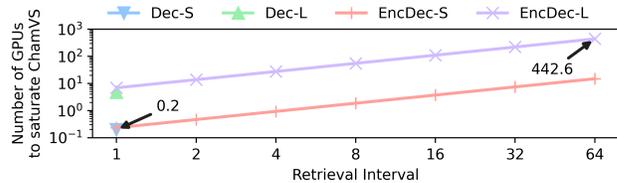


Figure 13. The optimal accelerator ratio varies significantly for different RALM configurations.

Resource disaggregation. Resource disaggregation has become increasingly popular in data centers. CPUs, memory, storage, and accelerators are connected through a high-speed network [25], such that they can be combined according to system needs without overprovisioning any type of the resources [27, 56, 74, 75]. The flexible introduction of extra resources, such as remote memory, helps in system performance compared to servers with monolithic designs [7, 108].

Near data processing. Various literature has proposed to offload some computation workloads to a processor near or within memory or storage to reduce expensive data movements [24, 60, 76, 80, 90, 92, 95, 97]. Typical use cases include database systems [24, 51], big data processing [33, 53, 54], recommender systems [48, 49, 102], time series processing [26], and genome sequence analysis [77]. The processors near the data can be regular CPUs [5], vector processors [83], reconfigurable hardware [30, 61], or ASICs [77].

AI accelerators. GPUs are commonly used for deep learning acceleration nowadays [20, 42, 99]. Alternative specialized architectures have also been implemented on FPGAs [8, 28, 79, 84, 94, 110] and ASICs [31, 35, 55, 62, 93, 109]. These accelerators are often co-designed with algorithm relaxations such as neural network pruning and quantization [29, 36, 70, 71]. Compiler-based solutions are also necessary to reduce the programming effort to map tensor programs to the various hardware backends [16, 64].

Vector search on modern hardware. Exact nearest neighbor search can be accelerated not only on GPUs but also TPUs [19] and FPGAs [105]. For ANN search, the most popular GPU-accelerated library so far is Faiss [52], and there are several academic GPU implementations [17, 18, 101]. Lee et al. [65] study ASIC designs for IVF-PQ, and the simulation-based evaluation shows significant speedup over GPUs. A couple of works [50, 107] implement IVF-PQ on an FPGA, but their designs are constrained by either the limited HBM capacity or the slow CPU-FPGA interconnect. In contrast, Chameleon disaggregates IVF-PQ, with the index on GPUs and PQ codes on FPGA-based memory nodes, and employs the innovative hardware priority queue design to achieve high performance with little hardware resources. While graph-based vector search accelerators can achieve low latency [106], the memory footprint of graphs is too high at scale, requiring up to one TB of memory for

only one billion SIFT vectors, in contrast to 24 GB in our case. Apart from accelerator-based solutions, researchers also study modern storage for vector search. Hu et al. [40] propose to push down vector distance evaluation to NAND flash to reduce data movement. Ren et al. [89] suggest storing vectors in non-volatile memory to scale up graph-based ANN, while on-disk ANN has to be careful with I/O cost [15, 46, 67]. The emerging CXL technology has introduced another level of memory hierarchy as an option for ANN search [45].

8 Conclusion

Retrieval-augmented language models offer compelling advantages but also present unique system design challenges. To address these problems, we present Chameleon, an efficient RALM inference engine that integrates two proposed system design principles: accelerator heterogeneity and accelerator disaggregation. Our Chameleon prototype achieves up to 3.18× speedup in throughput compared to the state-of-the-art systems, paving the way for adopting the proposed design principles in future-generation RALM systems.

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